In the Claims:

Please amend claims 20, 22, 31, 32, 33, 53, 54, 55, 64, 65, and 66, as specified below. The current status of the claims follows:

1-19. (canceled)

20. (currently amended) A radio-frequency (RF) transceiver, comprising:

a first integrated-circuit device that includes a receiver analog circuitry configured to produce ~~a~~ at least one digital receive signal from an analog radio-frequency signal, the receiver analog circuitry having a plurality of signal lines that are configurable by a control signal configured to have at least a first state and a second state; and

a second integrated-circuit device that includes a receiver digital circuitry configured to accept the at least one digital receive signal from the receiver analog circuitry, the receiver digital circuitry having a plurality of signal lines that are configurable by the control signal,

wherein the signal lines of the receiver analog ~~receiver~~ circuitry are coupled to the signal lines of the receiver digital circuitry, and wherein the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry are configured as a serial interface when the control signal is in the first state, the serial interface comprising a plurality of data signals and a plurality of control signals, wherein the receiver digital circuitry includes a plurality of signal driver circuitries configured to provide the plurality of data signals and the plurality of control signals of the serial interface to the receiver analog circuitry when the control signal is in the first state.

21. (previously presented) The transceiver of claim 20, in which the receiver analog circuitry includes a plurality of data receiver circuitries configured to accept the plurality of data signals and the plurality of control signals from the receiver digital circuitry when the control signal is in the first state.

22. (currently amended) The transceiver of claim 21, in which the receiver digital circuitry includes an interface controller circuitry configured to cause a serial data-out from the receiver analog circuitry to be received within the receiver digital circuitry, the interface controller circuitry

further configured to cause the serial data-out within the receiver digital circuitry to be selectively provided to a baseband processor circuitry coupled to the second integrated-circuit device.

23. (original) The transceiver of claim 22, in which the plurality of data signals and the plurality of control signals comprise band-limited current signals.

24-30. (canceled)

31. (previously presented) The transceiver of claim 23, in which the receiver analog circuitry includes a multiplexer circuitry configured to provide a data signal to a data driver circuitry in response to a data transfer clock.

32. (previously presented) The transceiver of claim 31, in which the multiplexer circuitry is further configured to accept a pair of output signals from an analog-to-digital converter (ADC) circuitry within the receiver analog circuitry, and to provide as the data signal one of the output signals on alternating transitions of the data transfer clock.

33. (previously presented) The transceiver of claim 32, in which the receiver analog circuitry derives the data transfer clock from a clock signal provided by the receiver digital circuitry.

34-52. (canceled)

53. (previously presented) A method of interfacing a receiver digital circuitry and a receiver analog circuitry within a radio-frequency (RF) transceiver, comprising:

providing in a first integrated-circuit device the receiver analog circuitry having a plurality of signal lines that are configurable by a control signal configured to have at least a first state and a second state;

utilizing the receiver analog circuitry to produce at least one digital receive signal from an analog radio-frequency signal;

providing in a second integrated-circuit device ~~a~~ the receiver digital circuitry having a plurality of signal lines that are configurable by the control signal and are coupled to the signal lines of the receiver analog circuitry;

accepting in the receiver digital circuitry the at least one digital receive signal from the receiver analog circuitry; and

using a plurality of signal driver circuitries in the receiver digital circuitry to provide to the receiver analog circuitry a plurality of data signals and a plurality of control signals in a serial interface that is formed when the control signal is in ~~a~~ the first state.

54. (previously presented) The method of claim 53, which further comprises providing a plurality of data receiver circuitries within the receiver analog circuitry, wherein the plurality of data receiver circuitries is configured to accept the plurality of data signals and the plurality of control signals from the receiver digital circuitry when the control signal is in the first state.

55. (currently amended) The method of claim 54, which further comprises providing an interface controller circuitry within the receiver digital circuitry, wherein the interface controller circuitry is configured to cause a serial data-out from the receiver analog circuitry to be received within the receiver digital circuitry, and wherein the interface controller circuitry is further configured to cause the serial data-out within the receiver digital circuitry to be selectively provided to a baseband processor circuitry coupled to the second integrated-circuit device.

56. (previously presented) The method of claim 55, which further comprises providing the plurality of data signals and the plurality of control signals as band-limited current signals.

57-63. (canceled)

64. (previously presented) The method of claim 56, which further comprises providing a multiplexer circuitry within the receiver analog circuitry, wherein the multiplexer circuitry is configured to provide a data signal to a data driver circuitry in response to a data transfer clock.

65. (previously presented) The method of claim 64, which further comprises:

providing within the receiver analog circuitry an analog-to-digital converter circuitry (ADC) configured to provide a pair of output signals; and

using the multiplexer circuitry to provide as the data signal one of the output signals of the analog-to-digital converter circuitry on alternating transitions of the data transfer clock.

66. (previously presented) The method of claim 65, which further comprises deriving within the receiver analog circuitry the data transfer clock from a clock signal provided by the receiver digital circuitry.